

## Implementation of Binary DAC and Two step ADC Quantizer for CTDS using gpdk45nm

Mr.T.Satyanarayana<sup>1</sup>, Mr.K.Ashok<sup>2</sup>, Mr. A.Vamshidhar Reddy

\*Associate Professor, ECE Department, CMR Engineering College ,Hyderabad E-mail: satyant234@gmail.com

\*\*Associate. Professor & HOD in ECE Dept., Annamacharya Institute of Technology & Science, Hyderabad

\*\*\*Asst. Professor in ECE Dept., CMR Technical Campus, Hyderabad Email:avamshia@gmail.com

**Abstract**—Two techniques to improve the performance of continuous-time delta–sigma (CTDS) modulators are presented. A digital calibration technique is introduced to enable the use of binary current digital-to-analog converters (DACs) without dynamic element matching. Furthermore, a high-speed two-step analog-to-digital data converter quantizer is introduced to efficiently increase the resolution of the quantizer in CTDS modulators with high-sampling rates. A proof-of-concept prototype implemented in 45-nm CMOS shows that the proposed calibration technique can compensate for up to 5% of mismatch in the DAC elements. The modulator has a measured SNDR/SFDR of 60.3/74 dB for a sampling rate of 350 MS/s and oversampling ratio of 20, translating to an 8.75-MHz bandwidth. The total power consumption is 5.5 mW from a 1.6 V supply.

**Index Terms**—Continuous-time, delta–sigma modulator, self-calibration, two-step analog-to-digital data converter (ADC) using 45nm technology

### I. INTRODUCTION

CONTINUOUS-TIME delta–sigma (CTDS) modulators are an efficient option to realize medium-to-high resolution/ low-to-medium-bandwidth analog-to-digital data converters (ADCs). Current-mode digital-to-analog converters (DACs) are widely used as one of the building blocks in CTDS modulators. These DACs must be extremely linear to attain sufficient linearity for the modulator. Conventionally, single-bit DACs that are inherently linear are utilized in delta–sigma modulators. However, they are sensitive to clock jitter [1]. Furthermore, in single-loop delta–sigma modulators with high integrator gain to maximize the signal-to-noise ratio (SNR), they can result in an unstable output [2]–[4]. Accordingly, multibit DACs are required to attain less sensitivity to clock jitter [1] and stable operation with a good SNR in high-order modulators.

The inherent current-cell mismatches in the current-mode DACs of a multibit structure limit the linearity performance of the CTDS modulator. To mitigate this problem, dynamic element matching (DEM) techniques are usually utilized to shape the DAC element mismatch errors to high frequencies. A drawback of DEM is that the required shuffling of all DAC elements dramatically increases the circuit complexity as a function of the number of involved current cells [5]. This results in an excess loop delay (ELD) in the modulator's feedback path which can cause the DAC pulse to be shifted into the next clock cycle. This effectively increases the order of the loop filter, potentially destabilizing the modulator, and degrading its noise-shaping performance, particularly in high-speed CTDS modulators [6], [7].

A promising technique to substitute the DEM block is DAC calibration. There are limited reported works on DAC calibration in CTDS modulators [2], [8]–[11]. These techniques are reported for unary DAC structures. Thus, the complexity of these techniques (e.g., the number of switches and their control signals, the number of unit element in the layout, etc.) can significantly increase when applying the technique in a higher resolution DAC. This paper proposes a digital DAC self-calibration technique that can be used in binary current-mode DACs. The proposed calibration technique is a foreground method and requires no significant additional analog circuitry. The digital correction block used to implement the calibration is also very simple due to the limited number of correction coefficients necessary for the binary output of the modulator.

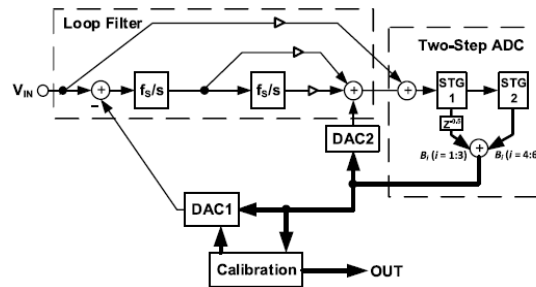


Figure 1. Architecture of the presented 350-MS/s CTDS modulator with digitally assisted binary-DAC calibration and a 5-bits two-step-ADC quantizer.

Traditionally, delta-sigma modulators utilize a unary DAC architecture, where the complexity is dramatically increased by the DAC resolution. However, the proposed DAC calibration allows the proposed CTDS modulator to employ a binary DAC architecture without DEM. Thus, due to the simplicity of the binary DAC cell, increasing DAC resolution becomes practical, and the resolution of the modulator's quantizer is also increased. Although flash ADCs are the common architecture to realize the quantizer, they require many comparators and a relatively large encoder, complicating the design of the quantizer. Alternatively, a two-step ADC quantizer is a good candidate to increase the quantizer's resolution without requiring many comparators and a large digital encoder (see [12], [13] in discrete-time modulators). Thus, in this paper, a multibit two-step-ADC quantizer, along with a foreground digital binary-DAC calibration technique, is introduced within the CTDS modulator.

As a proof-of-concept, a second-order CTDS modulator that utilizes the proposed techniques was implemented in 45nm CMOS technology. Section 1.1 presents the delta-sigma modulator architecture, while Section 1.2 details the two step- ADC quantizer. In Section IV, the binary-DAC calibration technique is proposed and detailed. Finally, Section V presents the measurement results of the implemented CTDS modulator.

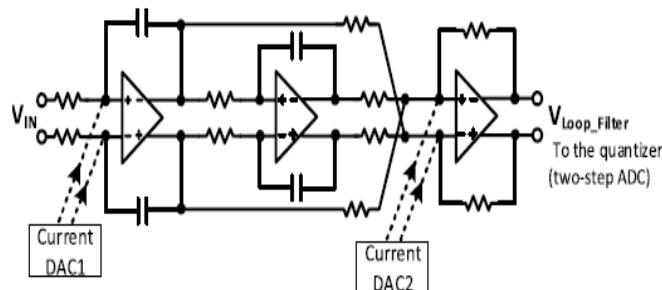


Figure 2. Circuit details of the utilized conventional second-order continuous time loop filter consisting of two integrators and a resistive adder.

### a. DELTA-SIGMA MODULATOR ARCHITECTURE

The key contributions of this paper are: 1) the DAC calibration technique that mitigates the need for DEM; and 2) the two-step ADC that allows for increased quantizer resolution. As such, a conventional second-order feed forward continuous time loop filter is employed in the CTDS modulator, as shown in Fig. 1. In the loop-filter of the modulator, the integrators are realized using op-amp-based RC integrators. The adder in front of the quantizer is an op-amp-based resistive adder. All op-amps have a telescopic structure to minimize their power and enhance their speed. The input is also directly added to the quantizer input in order to minimize the swing requirement of the adder's op-amp. Note that this addition is performed directly at the quantizer after the adder, as seen in Fig. 1. Fig. 2 shows the circuit details of the loop filter. The two-step ADC quantizer has a 5-bit resolution with one redundant bit, as described in Section 1.2. The conventional feedback path is closed through DAC1, which is a binary current nonreturn-to-zero (NRZ) DAC that is calibrated as detailed in Section 2.

The ELD which is a timing delay in the feedback DAC pulse results from the finite time required for the two-step- ADC quantizer to resolve its input and for the DAC1 to respond to the ADC output. This timing delay can cause the DAC pulse to be shifted into the next clock cycle which can potentially destabilize the modulator and degrade its noise-shaping performance [6], [7]. Here, the ELD can be compensated for by modifying the feed forward coefficients and introducing an additional feedback path through DAC2 from the modulator output to the input of the quantizer, as shown in Fig. 1 [7]. DAC2 is also a binary current NRZ DAC,

but it requires no calibration, as its errors are shaped by the loop filter in a similar fashion to the well-known shaping of quantization noise in the modulator.

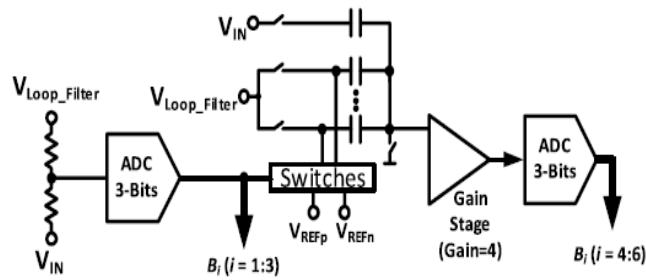


Figure 3. Five-bit two-step-ADC quantizer with 1-bit redundancy. The addition of the modulator’s input to the loop filter output is also shown. Note that a single-ended architecture is shown for simplicity.

In the primary design of the modulator, the equivalent discrete-time noise transfer function (NTF) of this second-order CTDS modulator is considered to be

$$NTF(z) = (1 - z^{-1})^2 \text{-----} (1)$$

The impulse-invariant transform is used to synthesize the equivalent continuous-time transfer function of this NTF [6]. A methodology for determining the feedforward coefficients and the additional feedback coefficient through DAC2 is presented in [6].

### b. TWO-STEP ADC QUANTIZER

Flash ADCs are widely utilized to realize the quantizer in delta-sigma modulators. However, in high-resolution implementations, the complexity of this ADC is exponentially increased. Every extra bit in such a quantizer doubles its complexity and power consumption, as well as the capacitive load of the analog circuit that drives the quantizer [1]. Accordingly, a two-step ADC quantizer is a good candidate to increase the quantizer’s resolution without requiring many comparators (less loading effect) and a complex digital encoder. Such an ADC has previously been utilized in discrete-time modulators at lower sampling frequencies [7], [8]. In this paper, a high speed two-step ADC is employed to realize the quantizer of the continuous-time modulator. Fig. 3 shows the two-step ADC which consists of two stages each having a 3-bit resolution. One redundant bit is present to relax the offset requirement of the comparators in the first stage. Thus, the total resolution of the quantizer is of 5 bits. The first stage is a standard switched-capacitor pipeline stage with six comparators and an acapacitor-based residue stage. The addition of the modulator’s input signal at the quantizer’s input seen in Fig. 1 is performed on the input capacitors of this residue stage, as shown in Fig. 3. In the residue stage, an open-loop gain stage is utilized to enhance the speed [14]. To reduce power consumption, no explicit sample and hold circuit is used. Note that the 1-bit redundancy also allows for the proposed low-complexity

Transition behavior of all switches phases,  $\phi$ . calibration technique, as described in Section 2. Note that as shown in Fig. 1, in order to synchronize the output bits of the two-step ADC, the output bits of its first stage (i.e., B1–B3) are delayed by a half clock cycle until the output bits of its second stage (i.e., B4–B6) are ready.

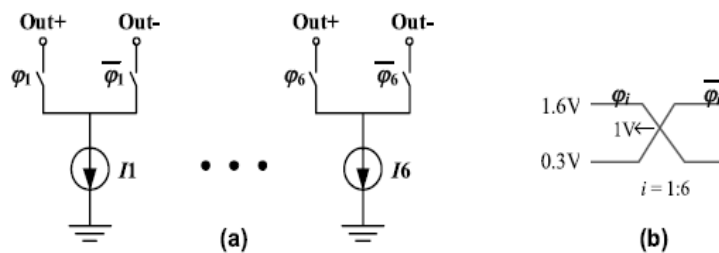


Fig. 4. (a) Utilized binary current DAC with  $I_1 = I_{REF}$ ,  $I_2 = I_{REF}/2$ ,  $I_3 = I_4 = I_{REF}/4$ ,  $I_5 = I_{REF}/8$ , and  $I_6 = I_{REF}/16$ . During the normal operation of the modulator, phases  $\phi_1 - \phi_6$  are connected to B1–B6, respectively. During the DAC calibration, these phases are connected as detailed in Table I. (b)

One of the merits of utilizing a two-step architecture is that the total quantizer delay is only slightly more than half a clock cycle. Accordingly, the instability effects resulting from this relatively short ELD can be readily compensated using direct feedback through DAC2 in front of the quantizer [6], [7]. Usually, an ELD that is larger than one clock cycle is avoided since its compensation requires more complex techniques [15].

### c. DIGITAL CALIBRATION OF BINARY-DAC ERRORS

Traditionally, DAC nonlinearity error correction techniques in delta-sigma modulators are mostly based on error shaping (i.e., DEM techniques) [16]. Although these techniques are very reliable, they do not shape the DAC errors efficiently at low oversampling ratios (OSRs) [2], and they result in an extra delay in the modulator's feedback path, degrading modulator stability. Another technique to mitigate the DAC nonlinearity is calibration. Recently, different DAC calibrations in CTDS sigma modulators have been proposed particularly in low OSR modulators [2], [8]–[11]. These techniques are reported for unary DAC structures, and as such their complexity (e.g., the number of switches and their control signals, the number of unit element in the layout, etc.) can noticeably increase by the DAC resolution.

Alternatively, the digital calibration technique proposed here applies to binary current DACs and requires almost no extra analog circuitry. Note that the proposed calibration is a self-calibration technique, since it utilizes the modulator itself to estimate the coefficient errors, which can lead to reduced area and power consumption. The digital correction block of this technique is also very simple due to the limited number of correction coefficients needed. Fig. 4(a) shows the utilized binary current DAC comprising of six switched current sources labeled from  $I_1$  to  $I_6$ . Fig. 4(b) shows the transition behavior of all switch phases,  $\phi$ . Here, all switch phases and their inverses are overlapped by utilizing reduced-swing high-crossing current switch drivers to minimize clock feed through effect and transient glitch energy [3], [17]. During the normal operation phase of the modulator, switch phases  $\phi_1$ – $\phi_3$  of binary-weighted current sources  $I_1$ – $I_3$  are controlled by the output bits of the first stage of the two-step-ADC quantizer (i.e.,  $B_1$ – $B_3$ ), while switch phases  $\phi_4$ – $\phi_6$  of binary-weighted current sources  $I_4$ – $I_6$  are controlled by the output bits of the second stage of the quantizer (i.e.,  $B_4$ – $B_6$ ). Here, the current of source  $I_3$  is equal to that of source  $I_4$  because of the 1-bit redundancy in the two-step-ADC quantizer. The proposed foreground calibration technique estimates the relative values of current sources  $I_2$ – $I_6$  with respect to that of  $I_1$  such that, in the digital domain, the relative bits of each current source is corrected using the estimated values.

In the calibration phase of the DAC, the input to the modulator is set to zero. Then, the values of switch phases  $\phi_2$ – $\phi_6$  of the DAC current sources are set to constant binary values. Only  $\phi_1$  is connected to the output of the quantizer (i.e.,  $B_1$ ). This is analogous to having a single output modulator (i.e.,  $B_1$ ), where  $\phi_2$ – $\phi_6$  control a current offset value,  $I_{OS}$ , at the output of the DAC. This current can also be converted to a voltage offset at the input of the modulator. Since the input of the modulator is zero, the average of the modulator's output (i.e.,  $B_1$ ) is relative to the offset value set by  $\phi_2$ – $\phi_6$ .

A typical calibration sequence for source  $I_2$  is described in order to illustrate the method. First,  $B_2$  is set to  $-1$  and the mean value of  $B_1$  ( $MB_0$ ) is saved. Then,  $B_2$  is set to  $+1$ , and the mean value of  $B_1$  ( $MB_1$ ) is saved again. The difference between these two values (i.e.,  $MB_0$ – $MB_1$ ) is equal to  $I_2/I_1$ . This is explained by the fact that when  $B_2$  goes from  $-1$  to  $+1$ , the offset current  $I_{OS}$  increases by  $I_2$ , and this offset is canceled at the DAC output by the resulting increase in the ON-time of current source  $I_1$  (i.e., the code density of  $B_1 = 1$  is increased in relation to  $I_2/I_1$ ). For added detail, the mathematical calculations of this calibration method are presented in the Appendix. Using the same procedure, the relative values of the other current sources with respect to that of  $I_1$  can be estimated. Note that the offset value of the ADC does not affect this estimation since its value affects both  $MB_0$  and  $MB_1$ , and hence it is canceled when calculating  $MB_0$ – $MB_1$ .

During the calibration phase, the modulator effectively utilizes a 1-bit quantizer, which limits its output linear range. If the current source switches are not set properly such that  $MB_0$  and  $MB_1$  are symmetric (i.e.,  $MB_1 \approx -MB_0$ ), the value of either  $MB_0$  or  $MB_1$  can more likely become sufficiently large to come close to the output linear range of the modulator such that the value of  $MB_0$ – $MB_1$  will include some error. Accordingly, when a current source is under calibration, the other current source switches are set such that the values of  $MB_0$  and  $MB_1$  are symmetric to help estimate the values of  $MB_1$  and  $MB_0$  more accurately. This can be done by setting the current source switches as shown in Table I. Interestingly, this symmetry is made possible by the use of redundant bits  $B_3$  and  $B_4$  in the quantizer, and it could not be realized with a standard binary output.

As can be seen, this calibration technique does not add any extra analog circuitry to the ADC as only a few switches are added to the DAC, and do not affect its behavior during its normal operation. Note that a calibration technique based on similar toggling of the DAC unit elements is also presented in [18] for a discrete-time delta-sigma modulator. However, it utilizes extra DAC elements to estimate the coefficient errors, and not the modulator DAC itself. As demonstrated in Section 3, the proposed calibration technique can estimate a relatively large current-mismatch value of 5%.

Table-I States of all Phases  $\varphi_i$  During the DAC calibration

Current source under calibration	$\varphi_1$	$\varphi_2$	$\varphi_3$	$\varphi_4$	$\varphi_5$	$\varphi_6$
$I_2$	$B_1$	-1→+1	-1	-1	+1	+1
$I_3$	$B_1$	-1	-1→+1	+1	-1	+1
$I_4$	$B_1$	-1	+1	-1→+1	-1	+1
$I_5$	$B_1$	-1	-1	+1	-1→+1	+1
$I_6$	$B_1$	-1	-1	+1	+1	-1→+1

Table- II

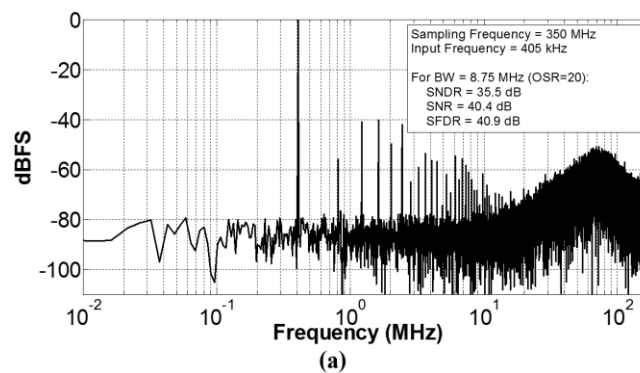
Estimated Values of the DAC Elements During Measurements Of a Typical Die Using The Proposed Calibration Technique

	$I_1/I_1$	$I_2/I_1$	$I_3/I_1$	$I_4/I_1$	$I_5/I_1$	$I_6/I_1$
Ideal Value	0.5	0.25	0.25	0.125	0.0625	
Estimated Value	0.4731	0.2533	0.2368	0.1233	0.06318	
Error (%)	-5.3	+1.3	-5.2	-1.3	+1.1	

#### d. MEASUREMENT RESULTS

The second-order CTDS modulator that utilizes the proposed techniques was implemented in a 45-nm CMOS technology. A chip micrograph is shown in Fig. 5. The circuitry occupies an active area of 260  $\mu\text{m} \times 300 \mu\text{m}$ . Measurements of this proof-of-concept prototype demonstrated that the proposed calibration technique can calibrate up to 5% of mismatch in the DAC elements. Note that, in this design, the DAC elements were sized intentionally small to be relatively highly mismatched. Table II shows the DAC mismatch values that were estimated using the proposed calibration technique.

As shown in Fig. 5(a) before calibration, the measurements of the modulator show an SNDR, SNR, and SFDR of 35.5, 40.4, and 40.9 dB, respectively, at an 8.75-MHz bandwidth (sampling rate of 350 MS/s and OSR of 20). As shown in Fig. 5(b), with the same bandwidth, the proposed calibration technique improves the SNDR, SNR, and SFDR values to 60.3, 62, and 74 dB, respectively. In addition, the modulator's dynamic range is 65 dB after calibration, as can be seen in Fig. 7. The total power consumption of the circuit is 5.5 mW from a 1.6-V supply voltage



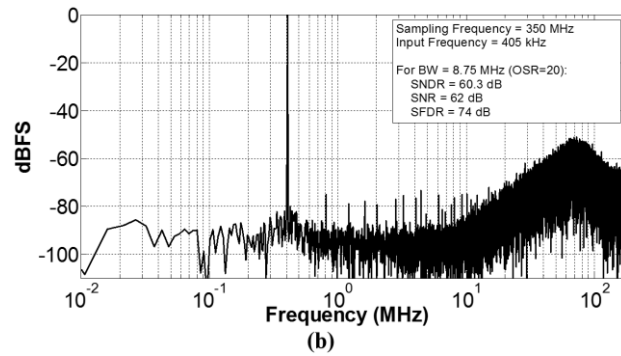


Fig. 6. Output spectrum of the presented CTDS modulator. (a) Before calibration. (b) After calibration.

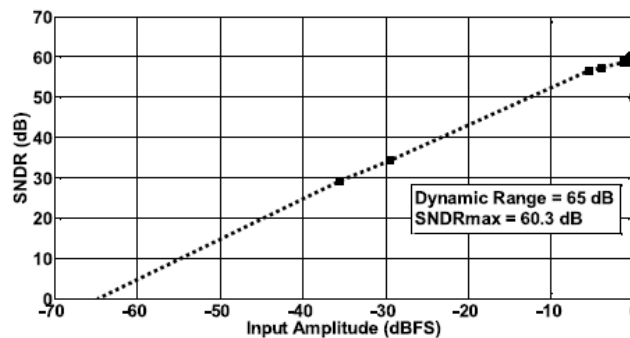


Fig. 6. Measured output SNDR versus the input amplitude of the modulator.

Table III lists the performance summary of the presented CTDS modulator, outlining its main conversion characteristics and its performance before and after calibration. Fig. 8 shows a comparison of the presented CTDS modulator to state-of-the-art CTDS modulators in 45nm CMOS. The following figure of merit (FOM) is used here:

$$FOM = \frac{Power}{2 \times BW \times 2^{ENOB}}$$

where BW represents the modulator bandwidth, and ENOB is the effective number of bits. Although the goal of this paper is to provide a proof-of-concept design for the two presented techniques, its FOM remains comparable with the state-of-the-art CTDS modulators in 45nm CMOS, while providing advantages with regards to design simplicity in the increased resolution quantizer and increased-resolution DAC, and with regards to robustness against high mismatch values in the DAC elements.

It should be noted that the modulator exhibits higher bandwidth and resolution in simulations. However, due to some unforeseen issues in its digital block, the sampling frequency had to be reduced. This reduction resulted in a lower modulator bandwidth, and also affected the noise shaping behavior of the modulator, which reduced the effective measured resolution. Furthermore, a few missing codes in the output of the two-step ADC were observed during measurements. This slight reduction in the quantizer's resolution, attributed to process variations, can lead to a reduced performance of the modulator. However, this is mitigated by the shaping of the quantizer's error by the loop filter, and its effect is accounted for in the measurement results.

TABLE III  
Performance Summary Of The Presented CTDS Modulator

Parameter	Value
Technology	45nm CMOS
Supply Voltage	1.6v
Sampling Frequency	350 MS/s
Input range	1.8v
SNDR /SFDR	31.5dB/50.9
SNR/ Dynamic Range	62dB/65db
Total Power Consumption	3.8mW



Total Area	260um x300um
FOM	0.3.1pJ/Conv-step

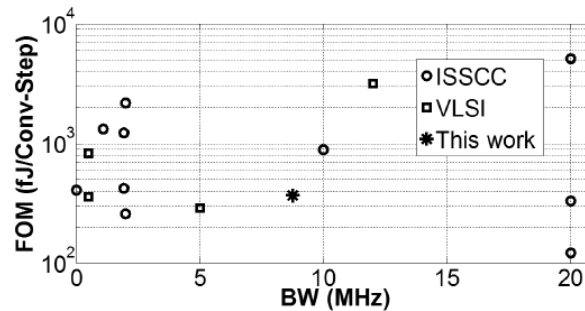


Fig. 7. Comparison of this work to state-of-the-art delta-sigma modulators implemented in 45nm CMOS that are reported in the International Solid-State Circuits Conference (ISSCC) or the Symposium on VLSI Circuits (VLSI) [19].

**e. CONCLUSION**

This paper presented a proof-of-concept prototype in 45nm CMOS to introduce two techniques to improve CTDS modulators. A low-complexity calibration technique is introduced to digitally estimate and correct the errors in a binary current DAC. Thus, no relatively complex DEM technique is required, and the related delay and power consumption increase are avoided. The proposed calibration technique can calibrate up to a 5% of mismatch in the DAC elements with very little added circuitry and additional active area. Furthermore, for CTDS modulators with high-sampling rates, a high-speed two-step-ADC quantizer is introduced to efficiently increase the modulator’s resolution. The modulator has a measured SNDR of 60.3 dB and an SFDR of 74 dB for a sampling rate of 350 MS/s and OSR of 20, translating to a 8.75-MHz bandwidth.

Ultimately, the CTDS modulator introduced in this paper enables the use of a low-complexity quantizer with increased resolution and of a DAC with increased resolution that is calibrated for high mismatch values in its elements.

**f. APPENDIX**

In summary, in the proposed DAC calibration technique, by two consecutive measurements in which the code of *B2* is toggled, the ratio of *I2/I1* is extracted. This Appendix aims at briefly presenting the mathematical details of the proposed calibration technique.

Toggling code *B2* from -1 to +1, is equivalent to adding an error signal to the DAC output with a normalized value of

$$E_{DAC} = \frac{2I_2}{I_{REF}} \text{ ----- (A.1)}$$

Where *IREF* is the differential reference current of the DAC. Since the DAC is a single-bit DAC with *IREF* = 2*I1*

$$E_{DAC} = \frac{I_2}{I_1} \text{ ----- (A.2)}$$

This error signal goes to the modulator’s output through the DAC error transfer function of

$$ETF(z) = \frac{H(z)}{1 + H(z)} \text{ ----- (A.3)}$$

where *H(z)* is the equivalent loop-filter transfer function (in discrete-time domain) of the modulator. Since during the calibration phase, *VIN* = 0, the modulator’s output is given by

$$\begin{aligned} OUT(z) &= NTF(z) \times Q_N(z) + ETF(z) \times E_{DAC} \\ &= \frac{1}{1 + H(z)} Q_N(z) + \frac{H(z)}{1 + H(z)} \frac{I_2}{I_1} \text{ ----- (A.4)} \end{aligned}$$

Where *QN* is the quantization noise of the quantizer. Considering a high low-frequency gain for *H*, the dc value of the modulator’s output is equal to *I2/I1*. Similar technique can be used to measure other current source values.

## II. ACKNOWLEDGMENT

The authors would like to thank Prof. A. Hamoui (deceased) from McGill University, Montréal, QC, Canada, for the fruitful discussions.

## REFERENCES

- [1] J. De Maeyer, P. Rombouts, and L. Weyten, "Efficient multibit quantization in continuous-time  $\Sigma\Delta$  modulators," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 54, no. 4, pp. 757–767, Apr. 2007.
- [2] J. G. Kauffman, P. Witte, J. Becker, and M. Ortmanns, "An 8.5 mW continuous-time  $\Sigma\Delta$  modulator with 25 MHz bandwidth using digital background DAC linearization to achieve 63.5 dB SNDR and 81 dB SFDR," *IEEE J. Solid-State Circuits*, vol. 46, no. 12, pp. 2869–2881, Dec. 2011.
- [3] S. Yan and E. Sánchez-Sinencio, "A continuous-time  $\Sigma\Delta$  modulator with 88-dB dynamic range and 1.1-MHz signal bandwidth," *IEEE J. Solid-State Circuits*, vol. 39, no. 1, pp. 75–86, Jan. 2004.
- [4] A. A. Hamoui and K. W. Martin, "High-order multibit modulators and pseudo data-weighted-averaging in low-oversampling  $\Sigma\Delta$  ADCs for broad-band applications," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 51, no. 1, pp. 72–85, Jan. 2004.
- [5] S.-C. Lee and Y. Chiu, "Digital calibration of capacitor mismatch in sigma-delta modulators," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 58, no. 4, pp. 690–698, Apr. 2011.
- [6] M. Ortmanns and F. Gerfers, *Continuous-Time Sigma-Delta A/D Conversion: Fundamentals, Performance Limits and Robust Implementations*. Berlin, Germany: Springer-Verlag, 2006.
- [7] F. Ali and A. A. Hamoui, "Continuous-time  $\Sigma\Delta$  modulators with noise-transfer-function enhancement," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2008, pp. 1428–1431.
- [8] C.-L. Lo, C.-Y. Ho, H.-C. Tsai, and Y.-H. Lin, "A 75.1 dB SNDR 840 MS/s CT  $\Sigma\Delta$  modulator with 30 MHz bandwidth and 46.4 fJ/conv FOM in 55 nm CMOS," in *Proc. IEEE Symp. VLSI Circuits*, Jun. 2013, pp. C60–C61.
- [9] X. Xing, M. De Bock, P. Rombouts, and G. Gielen, "A 40 MHz 12 bit 84.2 dB-SFDR continuous-time delta-sigma modulator in 90 nm CMOS," in *Proc. IEEE Asian Solid-State Circuits Conf.*, Nov. 2011, pp. 249–252.
- [10] M. De Bock, X. Xing, L. Weyten, G. Gielen, and P. Rombouts, "Calibration of DAC mismatch errors in  $\Sigma\Delta$  ADCs based on a sine wave measurement," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 60, no. 9, pp. 567–571, Sep. 2013.
- [11] Z. Li and T. S. Fiez, "A 14 bit continuous-time delta-sigma A/D modulator with 2.5 MHz signal bandwidth," *IEEE J. Solid-State Circuits*, vol. 42, no. 9, pp. 1873–1883, Sep. 2007.
- [12] O. Rajaei, S. Takeuchi, M. Aniya, K. Hamashita, and U.-K. Moon, "Low-OSR over-ranging hybrid ADC incorporating noise-shaped two step quantizer," *IEEE J. Solid-State Circuits*, vol. 46, no. 11, pp. 2458–2468, Nov. 2011.
- [13] O. Rajaei et al., "Design of a 79 dB 80 MHz 8X-OSR hybrid delta-sigma/pipelined ADC," *IEEE J. Solid-State Circuits*, vol. 45, no. 4, pp. 719–730, Apr. 2010.
- [14] B. Murmann and B. E. Boser, "A 12-bit 75-MS/s pipelined ADC using open-loop residue amplification," *IEEE J. Solid-State Circuits*, vol. 38, no. 12, pp. 2040–2050, Dec. 2003.
- [15] V. Singh, N. Krishnapura, S. Pavan, B. Vignanam, D. Behera, and N. Nigania, "A 16 MHz BW 75 dB DR CT  $\Sigma\Delta$  ADC compensated for more than one cycle excess loop delay," *IEEE J. Solid-State Circuits*, vol. 47, no. 8, pp. 1884–1895, Aug. 2012.
- [16] L. R. Carley, "A noise-shaping coder topology for 15+ bit converters," *IEEE J. Solid-State Circuits*, vol. 24, no. 2, pp. 267–273, Apr. 1989.
- [17] K. Falakshahi, C.-K. K. Yang, and B. A. Wooley, "A 14-bit, 10-Msamples/s D/A converter using multibit  $\Sigma\Delta$  modulation," *IEEE J. Solid-State Circuits*, vol. 34, no. 5, pp. 607–615, May 1999.
- [18] M. Sarhang-Nejad and G. C. Temes, "A high-resolution multibit  $\Sigma\Delta$  ADC with digital correction and relaxed amplifier requirements," *IEEE J. Solid-State Circuits*, vol. 28, no. 6, pp. 648–660, Jun. 1993.
- [19] B. Murmann. (2013). *ADC Performance Survey 1997–2013*. [Online]. Available: <http://www.stanford.edu/~murmman/adcsurvey.html>